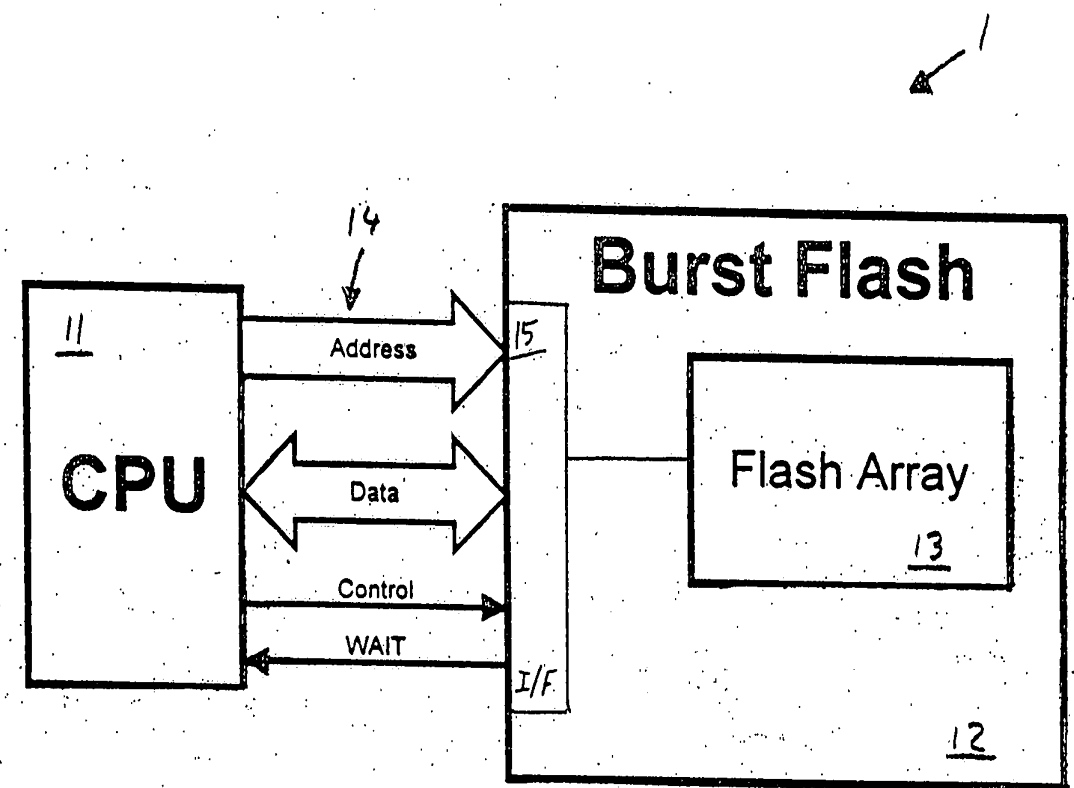

Fig. 1 - Prior Art

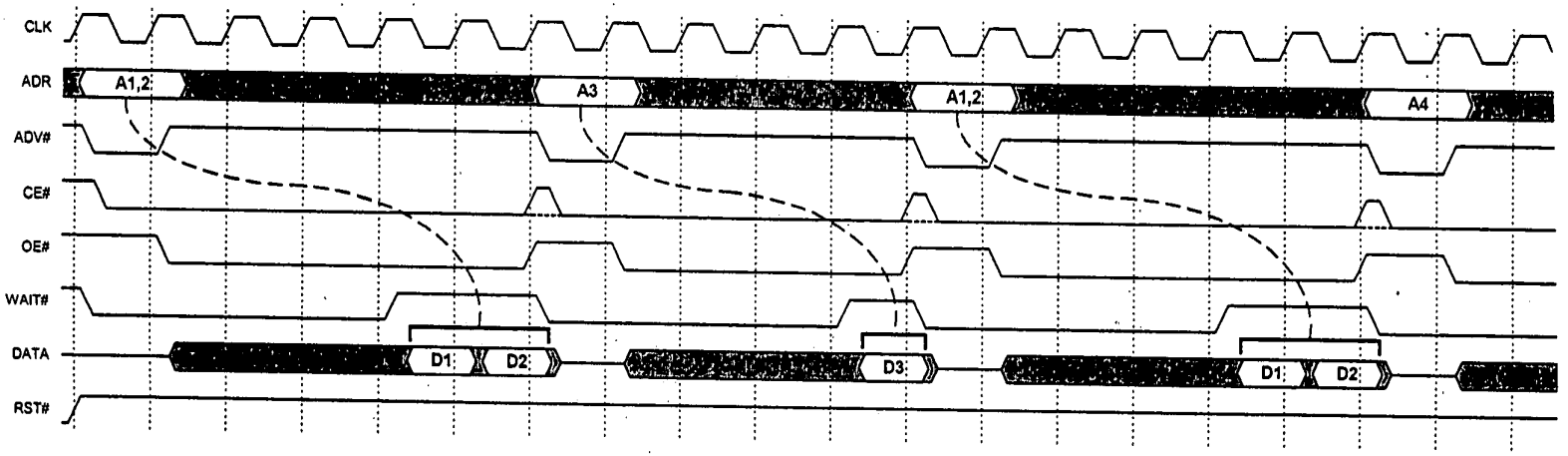

Fig. 2 - Prior Art

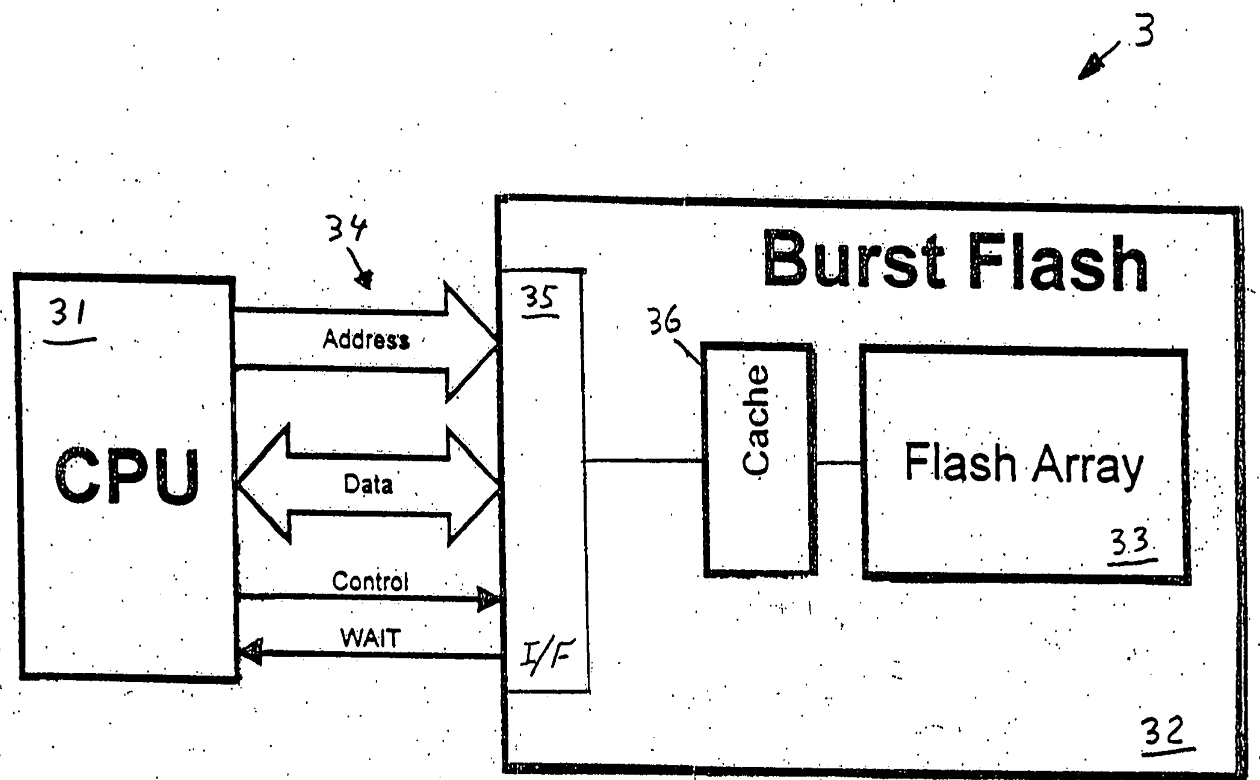

Fig. 3

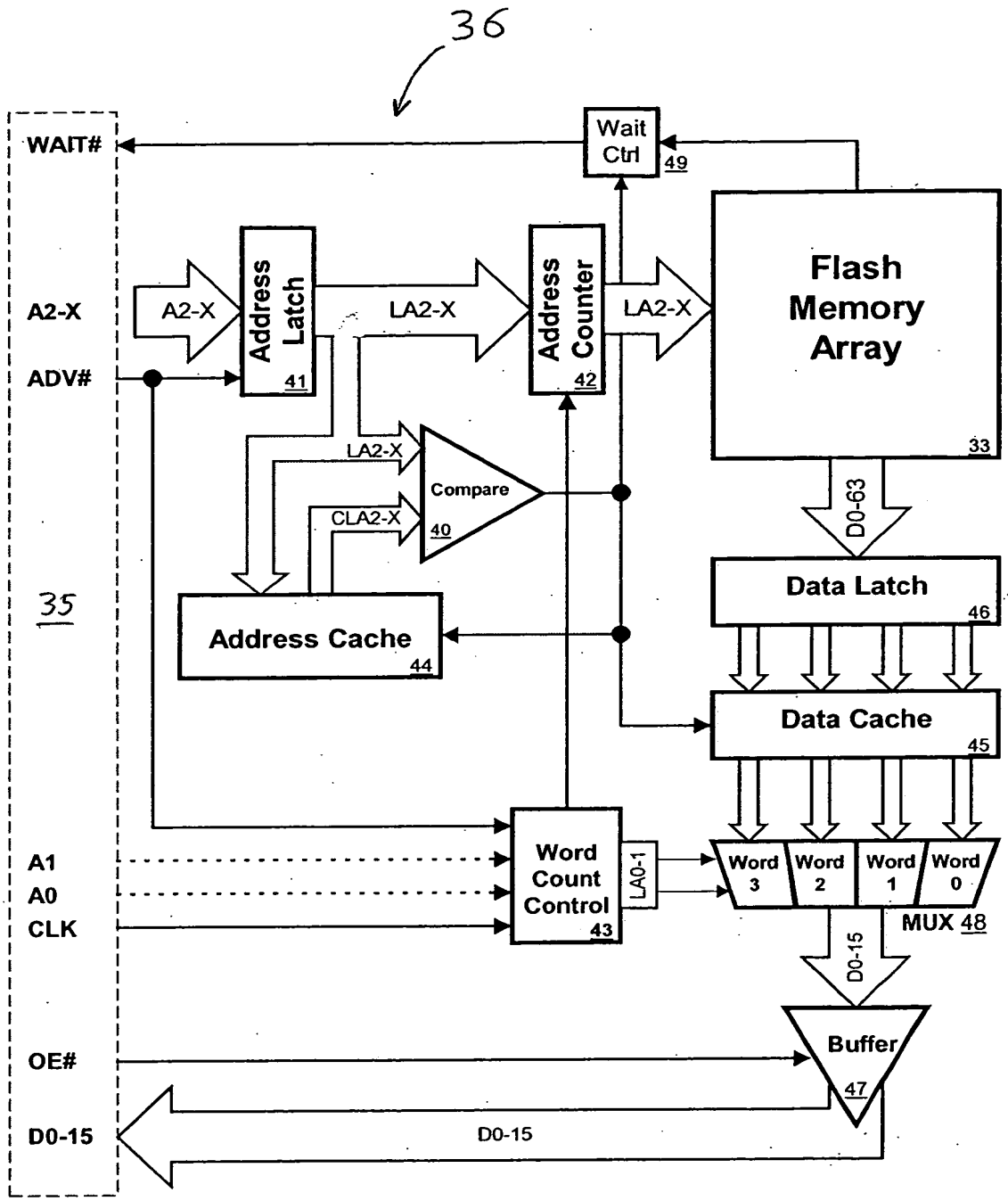
36
WAIT#
Wait Ctrl
49
A2-X
ADV#
A2-X
Address Latch
41
LA2-X
Address Counter
42
LA2-X
Flash Memory Array
33
LA2-X
CLA2-X
Compare
40
D0-63
Data Latch
46
35
Address Cache
44
Data Cache
45
A1
A0
CLK
Word Count Control
43
LA0-1
Word 3
Word 2
Word 1
Word 0
MUX 48
D0-15
Buffer
47
OE#
D0-15
D0-15

Fig. 4

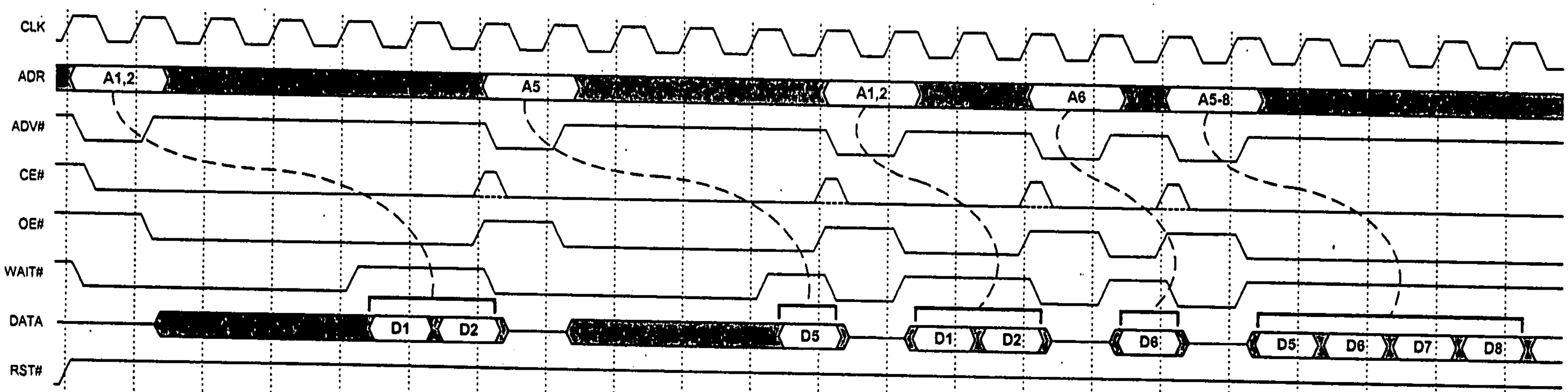
CLK
ADR
ADV#
CE#
OE#
WAIT#
DATA
RST#
A1,2
A5
A1,2
A6
A5-8
D1
D2
D5
D1
D2
D6
D5
D6
D7
D8

Fig. 5

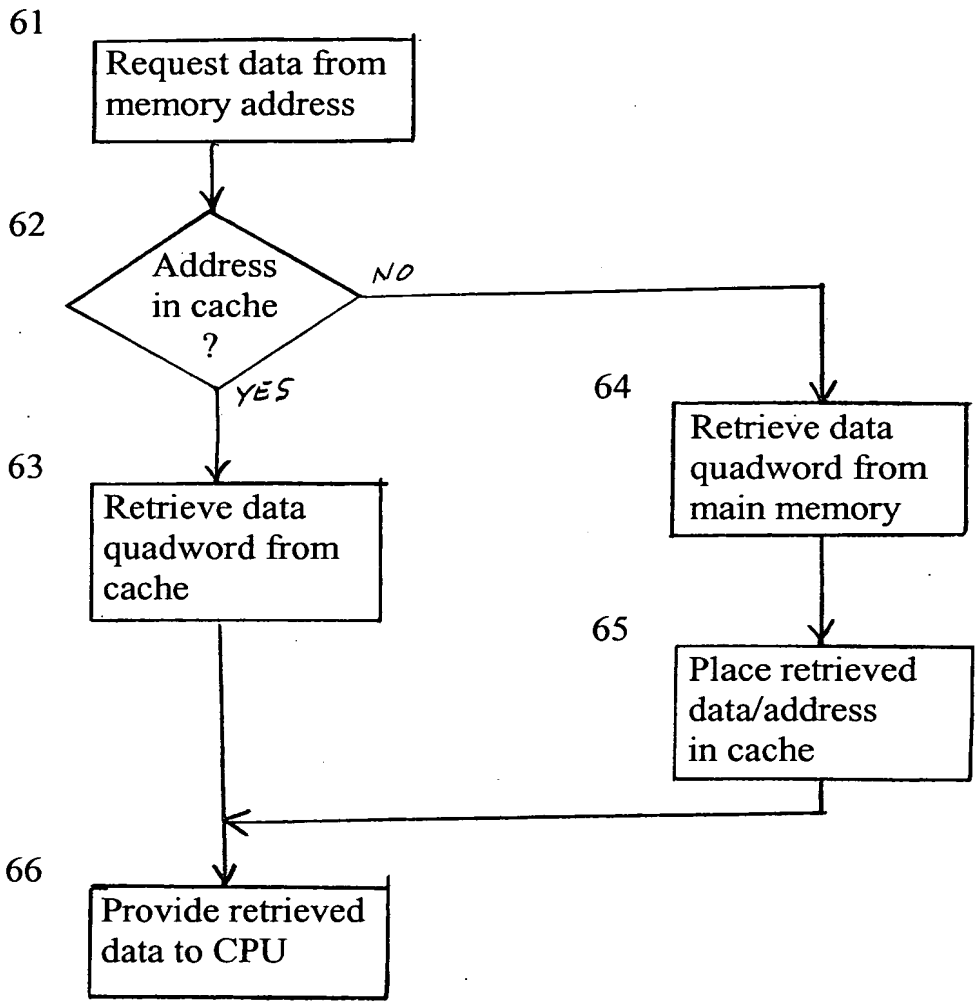
61
Request data from memory address
62
Address in cache ?
NO
YES
64
Retrieve data quadword from main memory
63
Retrieve data quadword from cache
65
Place retrieved data/address in cache
66
Provide retrieved data to CPU

Fig. 6

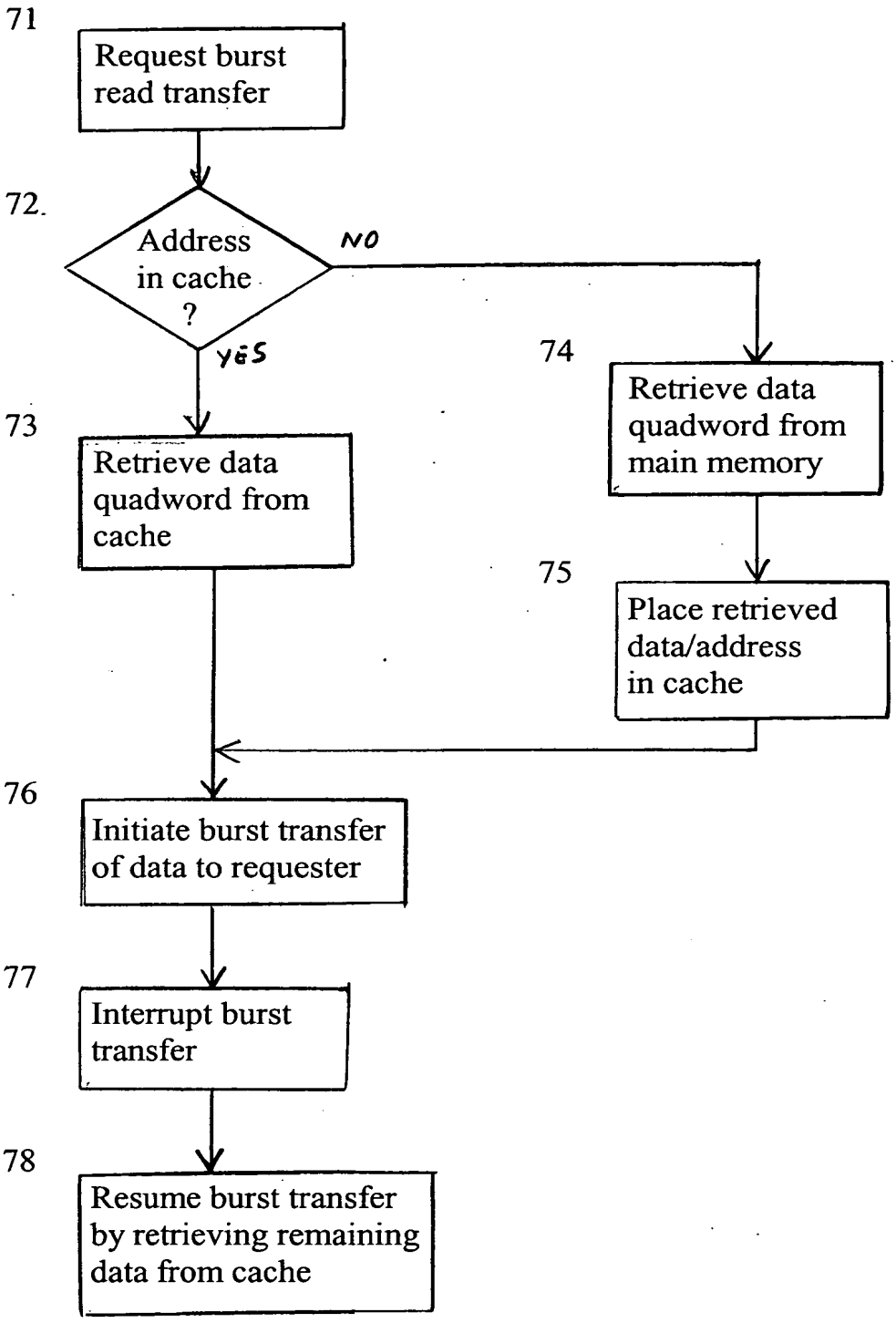
71
Request burst read transfer
72
Address in cache ?
NO
YES
74
Retrieve data quadword from main memory
73
Retrieve data quadword from cache
75
Place retrieved data/address in cache
76
Initiate burst transfer of data to requester
77
Interrupt burst transfer
78
Resume burst transfer by retrieving remaining data from cache

Fig. 7